

Department of Electronics and Telecommunication Engineering

COLLEGE OF ENGINEERING PUNE

(An Autonomous Institute of Government of Maharashtra)

Time Table

Class : S. Y. B. Tech E & TC
With Effect From : 08.11.2021

Academic Year : 2021 - 2022
Term : I (First)

Day TIME	9.00 am To 10.00 am	10.00 am To 11.00 am	11.00 am To 12.00 pm	12.00 pm To 1.00 pm	1.00 pm To 2.00 pm	2.00 pm To 3.00 pm	3.00 pm To 4.00 pm	4.00 pm To 5.00 pm	5.00 pm To 6.00pm
MON	LA & UC – DSY	FP – DSY S&S Tut (A) (SPMe)	S&S (SPMe)	Lunch Break	ODE & MVC (DNG)	NSAF (YDK)	EDC (A), DSD (B), CS (D), S&A (C), NSAF (E)		PLEVAH (Professional Laws, Ethics, Values and Harmony)
TUE	LA & UC – DSY	FP – DSY S&S Tut (B) (SPMe)	DSD (NRK)		ODE & MVC (DNG)	EDC (RPC)	EDC (E), DSD (A), CS (C), S&A (D), NSAF (B)		
WED	LA & UC – DSY	FP – DSY S&S Tut (C) (SPMe)	DSD (NRK)		S&S (SPMe)	EDC (RPC)	EDC (B), DSD (C), CS (E), S&A (A), NSAF (D)		
THU	LA & UC – DSY	S&A-IFC (SSK)	DSD (NRK)		NSAF (YDK)	EDC (RPC)	EDC (C), DSD (D), CS (B), S&A (E), NSAF (A)		
FRI		EDC (D), DSD (E), CS (A), S&A (B), NSAF (C)			ODE & MVC-TUT (DNG)	NSAF (YDK)	S&S Tut (D) (SPMe)	S&S Tut (E) (SPMe)	
SAT		I&C (Innovation and Creativity) (11.30 to 12.30 pm)							

Electronic Devices & Circuits (EDC) (Th + Lab): Mr. R.P. Chaudhari, **Digital System Design (DSD) (Th + Lab-Batches A, B ,C & D):** Ms. N. R. Kolhare,
Digital System Design (DSD) (Lab-Batch E): Dr. V. V. Ingale, **Signals & Systems (S&S) (Th + Tut):** Dr. Ms. S. P. Metkar,
Network Synthesis and Analog Filter (NSAF) (Th +Lab): Mrs. Y. D. Kapse,
Circuit Simulation (Lab-Batches A & B): Mr. G. K. Andurkar, **Circuit Simulation (Lab-Batches C, D & E):** Dr. Mrs. R. K. Patole
Sensors and Automation (S&A)(Th + Lab): Ms. Nikhila Patil (Instrumentation Dept.), **ODE & MVC (Th + Tut):** Mr. D. N. Ghayatadak (Mathematics Dept.)
For DSY: LA & UC (Th): (Mathematics Dept.), **Foundation of Physics (TH):** (Applied Science Dept.)

In-charge, Timetable Committee,
Department of Electronics & Telecommunication Engineering

Department of Electronics and Telecommunication Engineering

COLLEGE OF ENGINEERING PUNE

(An Autonomous Institute of Government of Maharashtra)

Time Table

Class : T. Y. B. Tech E & TC
With Effect From: 02.08.2021

Academic Year : 2021 - 2022
Term : I (First)

Day TIME	8.40 am To 9.40 am	9.50 am To 10.50 am	11.00 am To 12.00 pm	12.10 pm To 1.10 pm	1.10 pm To 1.40 pm	1.40 pm To 2.40 pm	2.50 pm To 3.50 pm	4.00 pm To 5.00 pm	5.10 pm To 6.10 pm	6.20 pm To 7.20 pm
MON		IFC - DA (VSI)	DSP (VSV)	PSE (CMD)	Lunch Break	DSP(A), DC(B), CLPD(C), DA(D), RPP(E) (1.40 pm to 3.40 pm)		CLPD Tut (A)	Minor (YMV)/ Honors (SGM)	
TUE		DC (VNM)	DSP (VSV)	PSE (CMD)		DSP(B), DC(C), CLPD(D), DA(E), RPP(A) (1.40 pm to 3.40 pm)		CLPD Tut (B)	Minor (YMV)/ Honors (SGM)	
WED	CLPD Tut (C)	DSP(C), DC(D), CLPD(E), DA(A), RPP(B) (10.00 am to 12.00 pm)		PSE-Tut (CMD)		CLPD (VVI)	EMWA (DVN)	DSP (VSV)	Minor (YMV)/ Honors (SGM)	
THU	COI (SSD)	DSP(D), DC(E), CLPD(A), DA(B), RPP(C) (10.00 am to 12.00 pm)		DC (VNM)		CLPD (VVI)	EMWA (DVN)	HSSOC (Humanities)	CLPD Tut (D)	
FRI	EPP ()	DSP(E), DC(A), CLPD(B), DA(C), RPP(D) (10.00 am to 12.00 pm)		DC (VNM)		CLPD (VVI)	EMWA (DVN)	HSSOC (Humanities)	CLPD Tut (E)	
SAT										

Configurable Logic and Processor Design (CLPD) (Th + Tut): Dr. Mrs. V. V. Ingale, **Digital Signal Processing (DSP) (Th + Lab):** Dr. Mrs. V. S. Vyas,
Configurable Logic and Processor Design (CLPD) (Lab): Dr. Mrs. V. S. Agarwal, **Digital Communication (DC) (Th + Lab):** Dr. Mrs. V. N. More
Electromagnetic Waves and Antennas (EMWA) (Th): Dr. Ms. D. V. Niture, **R and Python Programming (Lab):** Mr. R. V. Sadakale
Minor (Microcontrollers - Offered by E & TC dept.): Mrs. Y. M. Vaidya, **Honors (Random Signals and Stochastic Processes):** Mr. S. G. Mali
IFC - Internet of Things and Applications (offered by E & TC to Civil and Meta dept.): Dr. Mrs. R. C. Mahajan and Mr. P. P. Tasgaonkar

Probability and Statistics for Engineers (PSE)(Th): Dr. C. M. Deshpande, **Entrepreneurship Principles and Process (EPP)(Th):**

IFC - Data Analytics (DA)(Th + Lab-Batches D & E): Dr. Mrs. V. S. Inamdar, **IFC – Data Analytics (DA)(Lab-Batches A, B & C):** Mrs. A. S. Matange

Constitution of India (COI)(Th): Mrs. S. S. Deshpande

In-charge, Timetable Committee,
Department of Electronics & Telecommunication Engineering

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COLLEGE OF ENGINEERING PUNE

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Time Table

Class : **Final Year B. Tech E & TC**
With Effect From: 02.08.2021

Academic Year : 2021 - 2022
Term : I (First)

Day TIME	8.40 am To 9.40 am	9.50 am To 10.50 am	11.00 am To 12.00 pm	12.10 pm To 1.10 pm	1.10 pm To 1.40 pm	1.40 pm To 3.40 pm	4.00 pm To 5.00 pm	5.10 pm To 6.10 pm	6.20 pm To 7.20 pm
MON				DE-II RISC (SPMe)/ SP (RKP)/ DCMOS (PPS)	Lunch Break	AVE(A), CN(B), MOC(C), SP(E)	Honors (MSS)	Minor (RDJ)	
TUE			MOC (AGA)	DE-II RISC (SPMe)/ SP (RKP)/ DCMOS (PPS)		AVE(B), CN(C), MOC(D), DCMOS(A)	Honors (MSS)	Minor (RDJ)	
WED	ILOE	AVE (GKA)	CN (RAP)	DE-II RISC (SPMe)/ SP (RKP)/ DCMOS (PPS)		AVE(C), CN(D), MOC(E), SP(D)	Honors (MSS)	Minor (RDJ)	
THU	ILOE	AVE (GKA)	MOC (AGA)	CN (RAP)		AVE(D), CN(E), MOC(A), RISC(B)			
FRI	ILOE	AVE (GKA)	MOC (AGA)	CN (RAP)		AVE(E), CN(A), MOC(B), SP(C)			LLC
SAT									

Audio Video Engineering (AVE) (Th + Lab): Mr. G. K. Andurkar, **Microwave and Optical Communication (MOC) (Th + Lab):** Mrs. A. G. Andurkar
Computer Networks (CN) (Th + Lab Batches-A and E): Dr. R. A. patil

Department Elective - II:

RISC Microcontrollers and DSP Processors (RISC) (Th + Lab): Dr. Ms. S. P. Metkar, **Digital CMOS Design (DCMOS) (Th + Lab):** Dr. Mrs. P. P. Shingare

Honors (Advances in Digital Communication): Prof. M. S. Sutaone, **Minor (Wireless Sensor Networks – Offered by E & TC dept.):** Dr. R. D. Joshi

Institute Level Open Elective (ILOE) - Broadband Communication (Offered by E & TC dept.): Mr. R. V. Sadakale, **Liberal Learning Course (LLC):**

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