**College of Engineering, Pune**
**(An Autonomous Institute of Govt. of Maharashtra, Permanently Affiliated to S.P. Pune University)**

**Department of Electronics and Telecommunication**
**(Digital Systems)**

# Curriculum Structure & Detailed Syllabus (PG Program)
# M. Tech. - Electronics
**(Effective from: A.Y. 2019-20)**

**PG Program [M. Tech. Electronics –Digital Systems] Curriculum Structure**

**w.e.f. A. Y. 2019-20 and applicable for batches admitted from AY 2019-20**

## List of Abbreviations

| Abbreviation | Title | No of courses | Credits | % of Credits |
|---|---|---|---|---|
| PSMC | Program Specific Mathematics Course | 1 | 4 | 5.9% |
| PSBC | Program Specific Bridge Course | 1 | 3 | 4.4% |
| DEC | Department Elective Course | 3 | 9 | 13.2% |
| MLC | Mandatory Learning Course | 2 | - | 0% |
| PCC | Program Core Course | 5 | 15 | 22.0% |
| LC | Laboratory Course | 6 | 9 | 13.2% |
| IOC | Interdisciplinary Open Course | 1 | 3 | 4.4% |
| LLC | Liberal Learning Course | 1 | 1 | 1.5% |
| SLC | Self Learning Course | 2 | 6 | 8.8% |
| SBC | Skill Based Course | 2 | 18 | 26.5% |
| Total | | 24 | 68 | 100% |

**PG Program [M. Tech. Electronics –Digital Systems] Curriculum Structure**

**Semester I**

| Sr. No. | Course Type | Course Code | Course Name | Teaching Scheme | | | Credits |
|---|---|---|---|---|---|---|---|
| | | | | L | T | P | |
| 1. | PSMC | ETC-19002 | Probability, Graph and Field Theory | 3 | 1 | -- | 4 |
| 2. | PSBC | EDE-19012 | Processor Architectures | 3 | 0 | -- | 3 |
| 3. | DEC | EDE(DE)-19007<br>ETC(DE)-19004<br>ETC(DE)-19011<br>ETC(DE)-19005 | Department Elective I –<br>a) Image Processing and Computer Vision<br>b) Machine Learning<br>c) Modeling, Simulation and Optimization<br>d) Automotive Embedded Product Development ** | 3 | -- | -- | 3 |
| 4. | MLC | ML-19011 | Research Methodology and Intellectual Property Rights | 2 | -- | -- | -- |
| 5. | MLC | ML-19012 | Effective Technical Communication | 1 | -- | -- | -- |
| 6. | PCC | EDE-19013 | Digital Design and Verification | 3 | -- | -- | 3 |
| 7. | PCC | EDE-19014 | Artificial Intelligence | 3 | -- | -- | 3 |
| 8. | LC | EDE-19015 | Digital Design and Verification Laboratory | -- | 1 | 2 | 2 |
| 9. | LC | EDE-19018 | Artificial Intelligence Laboratory | -- | -- | 2 | 1 |
| 10. | LC | EDE-19016 | Simulation Laboratory | -- | 1 | 2 | 2 |
| 11. | LC | EDE-19017 | Seminar | -- | -- | 2 | 1 |
| | | | Sub Total | 18 | 3 | 8 | 22 |
| **Total Credits** | | | | **22** | | | |

*Note: ** Indicates Electives offered by HELLA, India*

Interdisciplinary Open Course (IOC): Every department shall offer one IOC course (in Engineering/Science/Technology). A student can opt for an IOC course offered by a department except the one offered by his /her department.

**Semester II**

| Sr. No. | Course Type | Course Code | Course Name | Teaching Scheme | | | Credits |
|---|---|---|---|---|---|---|---|
| | | | | L | T | P | |
| 1. | IOC | ETC-19004 | Interdisciplinary Open Course | 3 | -- | -- | 3 |
| 2. | DEC | ETC(DE)-19007<br>EDE(DE)-19002<br>EDE(DE)-19010<br>ETC(DE)-19001 | Department Elective –II<br>a) Automotive Electronics<br>b) Pattern Recognition and Classification<br>c) Blockchain Technology<br>d) Automotive Embedded Hardware Development ** | 3 | -- | -- | 3 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 3. | DEC | ETC(DE)-19008<br>EDE(DE)-19005<br>EDE(DE)-19006<br>ETC(DE)-19002 | Department Elective –III<br>a) Low power VLSI<br>b) Multimedia Systems<br>c) Fault Tolerant & Dependable Computing Systems<br>d) Automotive Embedded Software Development ** | 3 | -- | -- | 3 |
| 4. | LLC | LL-19001 | Liberal Learning Course | 1 | -- | -- | 1 |
| 5. | PCC | EDE-19002 | Embedded Systems Security | 3 | -- | -- | 3 |
| 6. | PCC | EDE-19003 | Real Time Operating Systems | 3 | -- | -- | 3 |
| 7. | PCC | EDE-19004 | Digital CMOS VLSI Design | 3 | -- | -- | 3 |
| 8. | LC | EDE-19005 | Real Time Operating System Laboratory | -- | -- | 2 | 1 |
| 9. | LC | EDE-19006 | Digital CMOS VLSI Design Laboratory | -- | -- | 2 | 1 |
| 10. | LC | EDE-19007 | Embedded Systems Security Laboratory | -- | -- | 2 | 1 |
| | | | Sub Total | 19 | -- | 6 | 22 |
| **Total Credits** | | | | 22 | | | |

*Note: ** Indicates Electives offered by HELLA, India*

Interdisciplinary Open Course on "Embedded System Design" is offered to students of other departments.

**Semester-III**

| Sr. No. | Course Type | Course Code | Course Name | Teaching Scheme | | | Credits |
|---|---|---|---|---|---|---|---|
| | | | | L | T | P | |
| 1. | SBC | EDE-20001 | Dissertation Phase – I | -- | -- | 18 | 9 |
| 2. | SLC | EDE-20002 | Massive Open Online Course –I | 3 | -- | -- | 3 |
| **Total** | | | | 3 | -- | 18 | 12 |

**Semester-IV**

| Sr. No. | Course Type | Course Code | Course Name | Teaching Scheme | | | Credits |
|---|---|---|---|---|---|---|---|
| | | | | L | T | P | |
| 1. | SBC | EDE-20003 | Dissertation Phase – II | -- | -- | 18 | 9 |
| 2. | SLC | EDE-20004 | Massive Open Online Course –II | 3 | -- | -- | 3 |
| **Total** | | | | 3 | -- | 18 | 12 |

*Massive Open Online Courses:*
*Depends on the Dissertation work, guides can decide appropriate subjects.*

*MOOC Courses Identified:*
- *Real Time Embedded Systems*
- *VLSI design for Fault Tolerance and Testability*
- *Parallel Computing*
- *Advanced IOT Applications*

**SEMESTER I**

## (PSMC) [ETC-19002] Probability, Graph and Field Theory

| Teaching Scheme | Examination Scheme |
|---|---|
| Lectures: 3 hrs/week | T1, T2 – 20 marks each, End-Sem Exam – 60 |
| Tutorials: 1 hr/week | Credits: 04 |

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Grasp and apply Graph theory for engineering problem solving and CAD tools developments
2. Culminate operations in groups, rings and field theory towards applications in digital electronic systems.
3. Characterize random variables and its functions with probability distributions and cumulative distributions

**Course Contents**:

**Graph Theory:**
Basic concepts of Graph Theory, Digraphs, Paths and Circuits, Reachability and Connectedness, Matrix representation of graphs, Subgraphs & Quotient Graphs, Isomorphic digraphs & Transitive Closure digraph, Euler's Path & Circuit- definitions and examples, Connected graphs and shortest paths: Walks, trails, paths, connected graphs, distance, cut-vertices, cut-edges, blocks, connectivity, weighted graphs, shortest path algorithms, Special classes of graphs: Bipartite graphs, line graphs, Chordal graphs, Planar graphs

**Group, Rings & Fields:**
Set theory Relations and Functions, Semigroups, Monoids, Subsemigroup, Submonoid, Isomorphism & Homomorphism, Fields, Integral Domain, Ring Homomorphism, Ring homomorphisms and their kernels, Ideals in commutative rings, First Isomorphism Theorem for commutative rings; the example of integers mod n, Abelian groups, Quotient Groups, fields of characteristic p > 0, algebraic field extension, algebraic closure, perfect field, Galois groups of polynomials, Galois groups over rationals,, Field automorphisms. Automorphism group, decomposition of a permutation into a product of disjoint cycles, Homological algebra, polynomials, Algebraic extensions, Galois extensions, Galois group of a polynomial. Galois correspondence, Calculating Galois groups. Cyclotomic extensions, Applications to Cryptography, Basic definitions of cellular automata and symbolic dynamics

**Probability and Statistics:**
Definitions, conditional probability, Bayes Theorem and independence. - Random Variables: Discrete, continuous and mixed random variables, probability mass, probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function, Chebyshev inequality. - Special Distributions: Discrete uniform, Binomial, Geometric, Poisson, Exponential, Gamma, Normal distributions. - Pseudo random sequence generation with given distribution, Functions of a Random Variable - Joint Distributions: Joint, marginal and conditional distributions, product moments, correlation, independence of random variables, bi-variate normal distribution. - Stochastic Processes: Definition and classification of stochastic processes, Poisson process - Norms, Statistical methods for ranking data

References:


1. Kolman, Bernard, Robert C. Busby, and Sharon Cutler Ross. Discrete mathematical structures. Prentice-Hall, Inc., 2003.
2. Dummit, David Steven, and Richard M. Foote. Abstract algebra. Vol. 3. Hoboken: Wiley, 2004.
3. McIntosh, Harold V. One dimensional cellular automata. Luniver Press, 2009.
4. Hoekstra, Alfons G., Jiri Kroc, and Peter MA Sloot, eds. Simulating complex systems by cellular automata. Springer, 2010.
5. Steeb, Willi-Hans. The nonlinear workbook: Chaos, fractals, cellular automata, genetic algorithms, gene expression programming, support vector machine, wavelets, hidden Markov models, fuzzy logic with C++. World Scientific Publishing Company, 2014.
6. Bondy, John Adrian, and Uppaluri Siva Ramachandra Murty. Graph theory with applications. Vol. 290. London: Macmillan, 1976.
7. Baron, Michael. Probability and statistics for computer scientists. Chapman and Hall/CRC, 2013.
8. Web Resources http://mathworld.wolfram.com/ElementaryCellularAutomaton.html


## (PSBC) [EDE-19012] Processor Architectures

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Identify and select the features, hardware and software both, supported by underlying embedded platform.
2. Determine the hardware blocks and control lines are used for specific instruction.
3. Analyse the system hardware against performance, and instruction throughput.

**Course Contents:**

**Parallel Processing and Pipelining Processing:** Architectural Classification, Applications of parallel processing, Instruction level Parallelism and Thread Level Parallelism, Explicitly Parallel Instruction Computing (EPIC) Architecture, Pipeline Architecture-Principles and implementation of Pipelining, Classification of pipelining processors, Design aspect of Arithmetic and Instruction pipelining, Pipelining hazards and resolving techniques, Data buffering techniques, Advanced pipelining techniques, Software pipelining, VLIW (Very Long Instruction Word) processor.

**Vector and Array Processor:** Issues in Vector Processing, Vector performance modelling, SIMD Computer

Organization, Static Vs Dynamic network, Parallel Algorithms for Array Processors: Matrix Multiplication.

**Multiprocessor Architecture:** Loosely and Tightly coupled multiprocessors, Inter Processor communication network, Time shared bus, Multiport Memory Model, Memory contention and arbitration techniques, Cache coherency and bus snooping, Massively Parallel Processors (MPP). Network on chip architectures.

**Multithreaded Architecture:** Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions, Parallel Programming Techniques: Message passing program development.

**Parallel algorithms for Multiprocessors:** Classification and performance of parallel algorithms, Operating systems for multiprocessors systems, Message passing libraries for parallel programming interface, PVM (in distributed memory system), Message Passing Interfaces (MPI). MIPS on FPGA

**DSP Architectures:** Parallelism in Digital Signal Processing. Digital Processing Architectures. The TMS320C2X Family. TMS320C25 –Overview

**References:**


1. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing" Mc-Graw Hill,
2. International Edition.
3. Kai Hwang, "Advanced Computer Architecture", McGraw-Hill, 1993.
4. William Stallings, "Computer Organization and Architecture, Designing for performance"Prentice Hall, Sixth edition.
5. Kai Hwang, "Scalable Parallel Computing". McGraw-Hill, 1998.
6. Harold S. Stone "High-Performance Computer Architecture". Addison-Wesley, 1993.
7. Tatas Konstantinos , Siozios Kostas, Soudris Dimitrios and Jantsch Axel, "Designing 2D and 3D Network-on-Chip Architectures." Springer, 2014.
8. TI User Manuals TMS320C2x
9. Smith, S. W. The Scientist and Engineer's Guide to Digital Signal Processing Marven, C., Ewers, G. A simple approach to DSP Texas Instr. 1993.


## (DEC-I) (a) [EDE(DE)-19007] - Image Processing and Computer Vision

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Understand fundamental concepts of digital image processing and computer vision.
2. Identify algorithms for enhancement, image analysis and restoration.
3. Analyze different techniques for segmentation, object recognition and compression.

**Course Contents:**

Concepts and techniques for image processing and computer vision; image representation,
**Enhancement:** enhancement by point processing, spatial filtering, enhancement in the frequency domain, Point, line detection, Edge detection, Edge linking, local processing, , Hough transform
**Segmentation**: boarder detection as graph searching, watershed segmentation, mean shift segmentation, active contour models, Thresholding, Iterative thresholding, Otsu's method, Region-based segmentation,
**Shape representation and description:** region identification, contour based shape representation
**Object recognition**: statistical pattern recognition,
**Restoration techniques:** Noise characterization, Noise restoration filters, Adaptive filters, Linear, Estimation of Degradation functions,
**Motion Analysis: Optical flow , detection of motion patterns**
**Compression:** Image and video compression

**References:**


1. Rafael C. Gonzalez and Richard E. Woods, "Digital Image Processing", Pearson, Third Edition, 2008.
2. Milan Sonka, V. Hlavac and Roger Boyle, Image Processing, Analysis and Machine Vision, Third edition, Thomson Asia Pvt. Ltd., 2008.
3. Anil K. Jain "Fundamentals of Digital image processing", PHI, 2010.
4. Forsyth, David A., Ponce, Jean, "Computer Vision: A Modern Approach" 2nd Edition, Pearson, 2012.
5. Madhuri A. Joshi, Mehul S. Raval, Yogesh H. Dandawate, Kalyani R. Joshi, Shilpa P. Metkar, "Image and Video Compression: Fundamentals, Techniques, and Applications", 1st Edition Chapman and Hall / CRC Published November 17, 2014 .


## (DEC-I) (b) [ETC(DE)-19004] - Machine Learning

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Design and implement machine learning solutions to a) Classification b) Regression c) Clustering problems
2. Evaluate and interpret the results of the machine learning algorithms

**Course Contents:**

Review of Probability Theory and Linear algebra, Convex Optimization, Introduction to Statistical Decision Theory, Regression: Linear Regression, Multivariate Regression, Subset Selection, Shrinkage Methods, Principal Component Regression, Logistic Regression, Partial Least Squares Classification:

Linear Classification, LDA Introduction to Perceptron and SVM, Neural Networks: Introduction, Early Models, Perceptron Learning, Back-propagation, Initialization of neural network, Training and Validation, Parameter Estimation Decision Trees - Stopping Criterion and Pruning, Loss function, Categorical Attributes, Multiway Splits, Missing values, Instability, Regression Trees. Bootstrapping and Cross Validation, Class Evaluation, Measures, ROC curve, MDL, Ensemble methods, Committee Machines and Stacking. Gradient Boosting, Random Forests, Multi-class Classification, Naïve Bayes, Bayesian Networks, Undirected Graphical Models, HMM, Variable elimination, Belief Propagation, Partitional clustering, Hierarchical Clustering, Birch Algorithm, CURE Algorithm, Density- Based Clustering, Gaussian Mixture Models, Expectation Maximization, Learning Theory, Re-enforcement Learning

**References:**


1. Ethem Alpaydin, "Introduction to Machine Learning", PHI, 2005
2. Bishop Christopher, "Neural Networks for Pattern Recognition", New York, NY: Oxford University Press, ISBN: 9780198538646
3. Mitchell Tom, "Machine learning", New York, NY: McGraw-Hill, ISBN:9780070428072
4. Hastie, T. R. Tibshirani, and J. G. Friedman, "The Elements of Statistical Learning: Data Mining, Inference and Prediction", New York, NY: Springer, ISBN:9780387952840
5. Gareth James, Daniela Witten, Trevor Hastie, Robert Tibshirani "Introduction to Statistical Learning", Springer, 2013.


## (DEC-I) (c) [ETC(DE)-19011] - Modeling, Simulation and Optimization

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes**:

At the end of the course, students will demonstrate the ability to:

1. Understand the steps of modelling and experimenting simulation.
2. Apply statistical knowledge and modelling techniques to construct simulation models
3. Interpret, analyze and simulation results using Simulation Programming Languages

**Course Contents:**

**Introduction to Computer Simulation:** Principles of Computer Modelling and Simulation, - Nature of Computer Modeling and Simulation, Continuous and Discrete Event types of simulation, Simulation as a decision making tool, Monte Carlo Simulation.

**Mathematical Techniques:** Random Numbers and Random Variables, Pseudo Random Numbers Techniques for Generating Random Numbers – Mid-Square method, Linear Congruential methods, Z-distribution, t-distribution, Tests for Random Numbers – Revision of Probability distributions, Uniform, Poisson, exponential, Inverse transform, Acceptance-Rejection methods, Relevant R-Programming exposure

**Continuous and Discrete Event Modelling and Simulation:** Representing complex system behavior through computer program framework using core concepts of entities, events, resources, queues disciplines. Input and Output modelling, Conceptual introduction to entity generator, ability to define attributes and variables, resource management and queue management capabilities, random delays and ability to terminate a simulation based on system state.

**Introduction to Simulation Languages:** Development of simulation models using simulation languages like GPSS and ARENA.

**Input Modelling and Output Analysis:** Trace Driven and parameric modelling, ARENA Input Analyzer, Terminating and Steady state simulation models, Statistics collection

**Network Optimization**: Continuous and Discrete Models: Overview of Network flow algorithm, Max-Flow and Min-Cost flow problem , Non linear Network optimization, Simulation Optimization overview, Response surface and neural nets, Optimization under uncertainty

**References:**


1. Sankar Sengupta, "System Simulation & Modeling" – Pearson Publs.
2. Jerry Banks and John S.Carson, Barry L. Nelson, David M. Nicol, "Discrete Event System Simulation", Prentice Hall, India.
3. Abhijit Gosavi, Simulation based optimization, Kluwer Academic
4. Tayfur Altiok, Benjamin Melamed, Simulation, Modeling and Analysis with ARENA
5. Urmila Diwekar, Introduction to Applied Optimization
6. Dimitri P. Bertsekas , Network Optimization: Continuous and Discrete Models,
7. B.P. Zeigler, H. Praehofer, T.G. Kim, "Theory of Modeling and Simulation"
8. R. Senthilkumar, P. Paneer selvam, System Simulation, Modeling and Languages, PHI
9. Kai Velten , Mathematical Modeling and Simulation-, Wiley-VCH


## (DEC-I) (d) [ETC(DE)-19005]- Automotive Embedded Product Development

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Acquire automotive product development understanding
2. Learn project management concept
3. Apply processes, methods and tools to demonstrate learning

**Course Contents:**

Automotive System Overview & Product development: Major Automotive trends (e-mobility, Autonomous Driving, Comfort & Connected Cars), Vehicle EE architecture, Products. Integration of Mechanical, Software, Hardware domains and their interdependences, Design for x Abilities (manufacturability, testability, serviceability, maintainability), Overview of Design guidelines.
Process, Methods & Tools: Requirements engineering and version control tools: DOORS, PTC, V model, Product Engineering Process, Automotive Spice, TS 16949, Key Performance Indicators for development.
Product Reliability, Safety and Quality: DFMEA, PFMES, Warranty, Design Validations, Process Validations, Customer Line Return, Non Quality Expenses, First Pass Yield, Statistical tools, ASIL levels, Safety Goals, Safety Measures, HARA, FMEDA, ISO 26262
Project Management and Organization: Matrix Organization, Line responsibilities, Functional responsibility, Team work, Leadership, Scope management, Scheduling, Cost, Monitoring & Tracking, Engineering Change Management, Milestones.

**References:**


1. Online resources
2. Reference manuals from Hella-India


## (MLC) [ML-19011] - Research Methodology and Intellectual Property Rights

**Teaching Scheme**
Lectures: 2 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 00

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Understand research problem formulation and approaches of investigation of solutions for research problems
2. Learn ethical practices to be followed in research and apply research methodology in case studies and acquire skills required for presentation of research outcomes
3. Discover how IPR is regarded as a source of national wealth and mark of an economic leadership in context of global market scenario
4. Summarize that it is an incentive for further research work and investment in R & D, leading to creation of new and better products and generation of economic and social benefits

**Course Contents:**

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations.

Effective literature studies approaches, analysis, Use Design of Experiments /Taguchi Method to plan a set of experiments or simulations or build prototype, Analyze your results and draw conclusions or Build

Prototype, Test and Redesign

Plagiarism, Research ethics, Effective technical writing, how to write report, Paper, Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Introduction to the concepts Property and Intellectual Property, Nature and Importance of Intellectual Property Rights, Objectives and Importance of understanding Intellectual Property Rights

Understanding the types of Intellectual Property Rights: -Patents-Indian Patent Office and its Administration, Administration of Patent System – Patenting under Indian Patent Act , Patent Rights and its Scope, Licensing and transfer of technology, Patent information and database. Provisional and Non Provisional Patent Application and Specification, Plant Patenting, Idea Patenting, Integrated Circuits, Industrial Designs, Trademarks (Registered and unregistered trademarks), Copyrights, Traditional Knowledge, Geographical Indications, Trade Secrets, Case Studies

New Developments in IPR, Process of Patenting and Development: technological research, innovation, patenting, development, International Scenario: WIPO, TRIPs, Patenting under PCT

**References:**


1. Aswani Kumar Bansal : Law of Trademarks in India
2. B L Wadehra : Law Relating to Patents, Trademarks, Copyright, Designs and Geographical Indications.
3. G.V.G Krishnamurthy : The Law of Trademarks, Copyright, Patents and Design.
4. Satyawrat Ponkse: The Management of Intellectual Property.
5. S K Roy Chaudhary & H K Saharay : The Law of Trademarks, Copyright, Patents
6. Intellectual Property Rights under WTO by T. Ramappa, S. Chand.
7. Manual of Patent Office Practice and Procedure
8. WIPO : WIPO Guide To Using Patent Information
9. Resisting Intellectual Property by Halbert ,Taylor & Francis
10. Industrial Design by Mayall, Mc Graw Hill
11. Product Design by Niebel, Mc Graw Hill
12. Introduction to Design by Asimov, Prentice Hall
13. Intellectual Property in New Technological Age by Robert P. Merges, Peter S. Menell, Mark A. Lemley


## (MLC) [ML-19012]- Effective Technical Communication Skills

**Teaching Scheme**
Lectures: 2 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 00

**Course Outcomes:**

At the end of the course, students will be able to:

1. Produce effective dialogue for business related situations
2. Use listening, speaking, reading and writing skills for communication purposes and attempt tasks by using functional grammar and vocabulary effectively
3. Analyze critically different concepts / principles of communication skills
4. Demonstrate productive skills and have a knack for structured conversations

5. Appreciate, analyze, evaluate business reports and research papers

**Course Contents:**

**Fundamentals of Communication**: 7 Cs of communication, common errors in English, enriching vocabulary, styles and registers

**Aural-Oral Communication**: The art of listening, stress and intonation, group discussion, oral presentation skills

**Reading and Writing**: Types of reading, effective writing, business correspondence, interpretation of technical reports and research papers

**References:**


1. Raman Sharma, "Technical Communication", Oxford University Press.
2. Raymond Murphy "Essential English Grammar" (Elementary & Intermediate) Cambridge University Press.
3. Mark Hancock "English Pronunciation in Use" Cambridge University Press.
4. Shirley Taylor, "Model Business Letters, Emails and Other Business Documents" (seventh edition), Prentise Hall
5. Thomas Huckin, Leslie Olsen "Technical writing and Professional Communications for Non-native speakers of English", McGraw Hill.


## (PCC) [EDE-19013] - Digital Design and Verification

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 3

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Analyse different combinational and sequential digital systems and its design methodology.
2. Design combinational and sequential digital systems using Verilog / System Verilog
3. Understanding of RTL design and verification techniques and methodologies.
4. Build the local eco-system in VLSI and Semiconductor field.

**Course Contents:**

**Revision of basic Digital systems:** Combinational Circuits, Sequential Circuits, Logic families. Synchronous FSM and asynchronous design, Metastability, Clock distribution and issues, basic building blocks like PWM module, pre-fetch unit, programmable counter, FIFO, Booth's multiplier, ALU, Barrel shifter etc.

**Verilog/VHDL Comparisons and Guidelines, Verilog:** HDL fundamentals, simulation, and test bench design, Examples of Verilog codes for combinational and sequential logic, Verilog AMS

**System Verilog and Verification:** Verification guidelines, Data types, procedural statements and routines, connecting the test bench and design, Assertions, Basic OOP concepts, Randomization, Introduction to basic scripting language: Perl, Tcl/Tk

**Current challenges in physical design:** Roots of challenges, Delays: Wire load models Generic PD flow, Challenges in PD flow at different steps, SI Challenge - Noise & Crosstalk, IR Drop,

**Process effects:** Process Antenna Effect & Electromigration Programmable Logic Devices: Introduction, Evolution: PROM, PLA, PAL, Architecture of PAL's, Applications, Programming PLD's, FPGA with technology: Antifuse, SRAM, EPROM, MUX, FPGA structures, and ASIC Design Flows, Programmable Interconnections,

**Coarse grained reconfigurable devices IP and Prototyping:** IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, and Use of external hard IP during prototyping, Case studies, and Speed issues. Testing of logic circuits: Fault models, BIST, JTAG interface

**References:**


1. Douglas Smith, "HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs Using VHDL or Verilog", Doone Publications 1998.
2. Samir Palnitkar, "Verilog HDL, A guide to Digital Design and Synthesis", Prentice Hall.
3. Doug Amos, Austin Lesea, Rene Richter, "FPGA based Prototyping Methodology Manual", Synopsis Press.
4. Christophe Bobda, "Introduction to Reconfigurable Computing, Architectures, Algorithms", Springer Netherlands.
5. Janick Bergeron, "Writing Testbenches: Functional Verification of HDL Model", Second Edition, Springer 2003.


## (PCC) [EDE-19014]- Artificial Intelligence

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 3

**Course Outcomes**:

At the end of the course, students will demonstrate the ability to:

1. Identify and formalize a given problem in the framework of solution by AI methods
2. Ability to design Fuzzy Logic based system for engineering applications
3. Understanding of major areas and challenges related to Inconsistent Information systems, Evolutionary Computing and Chaotic systems

**Course Contents:**

**Knowledge Representation:** Prepositional Logic, Inference Rules in Prepositional Logic, Knowledge representation using Predicate logic, AI Programming - Declarative versus procedural programming, introduction to LISP and PROLOG Predicate Calculus, Applications - Inference engine using PROLOG

**Inconsistent Information Systems:** Basic Concepts of Rough Sets, Equivalence Class and Discernibility Relations, Lower and Upper approximations, Information Systems Framework using Rough Sets, Reducts and Core, Introduction to Rough Set Software ROSE, Rules extractions, Missing Attributes computations, Instability analysis of Inconsistent Information Systems, Outsourcing Resource Selection using Rough set, Applications - Information Gain and data mining consideration

**Fuzzy Logic:** Representation and Manipulation of Imprecision and uncertainty :Fuzzy Sets, Type-I Membership Functions –Triangular, trapezoidal, PI, T-Norm, S-Norm Fuzzy Operations, Fuzzy Hedges, Convex combination of fuzzy sets, Fuzzy Relations & composition, Fuzzy Object Class, Applications - Fuzzy Logic Support in DoS commands, Email filters Documentation systems

**Engineering Adaptations of Fuzzy Systems:** Fuzzy Logic IC chips, Fuzzy Inference Engine and rule based systems, Fuzzy controllers, Stability computations, Embedded FuzzyControllers using DSP Chips, Decision Making with Fuzzy Information, Applications-Fuzzy Median Filters, Image processing on DSP platforms like TMS320C6713

**Non-linear Dynamical Systems and Chaos:** 1-D and 2-D Maps, cobweb diagrams, Fractals, Cantor set, Mandelbrot set, Chaotic orbits, Chaotic attractors, Bifurcations, delay coordinate and dimension embedding, Fractals, Commonly encountered mathematical fractals, Computer hardware systems as non-linear dynamic system

**Evolutionary Computing:** Genetic Algorithms, Schemata Representation, Introduction to Genetic programming, Examples using GA/GP, Application Optimization problems

**References :**


1. Fundamentals of the New Artificial Intelligence by Toshinori Munakata, Springer.
2. Artificial Intelligence: A Modern Approach by Stuart Russell & Peter Nerving, Prentice Hall
3. Artificial Intelligence by Elaine Rich, Kevin Knight, B. Nair, Tata Mc Graw Hill


## (LC) [EDE-19015] - Digital Design and Verification Laboratory

| Teaching Scheme | Examination Scheme |
|---|---|
| Tutorial: 1 hr/week | Marks: 100 |
| Practical: 2 hrs/week | Credits: 2 |

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Understand the programmable and reprogrammable systems
2. Identify, formulate, solve and implement problems in signal processing, communication systems

etc using RTL design tools.

**Course Contents**:

1. Designing combinational logic using MSI devices: Octal tristate buffer MUX/DeMUX , ALU, Priority encoder, Booths Multiplier
2. Designing sequential logic: Up/down counter, Barrel shifter, Memory model, Shift register, Bus arbitration logic, State machine/vending machine, RISC CPU
3. PCI Bus and Arbiter UART / USART implementation Realization of single port SRAM
4. Discrete Fourier transform or Fast Fourier Transform algorithm in verilog.

Note: Lab Journal: In the form of CD (Should contain Coding, snapshot of result, synthesis report, RTL view, pre & post synthesis and implementation reports)

## (LC) [EDE-19018]- Artificial Intelligence Laboratory

| Teaching Scheme | Examination Scheme |
|---|---|
| Practical: 2 hrs/week | Marks: 100 |
| | Credits: 1 |

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Implement the symbolic computation using PROLOG.
2. Understand and analyse parameters of Artificial Intelligence.

**Course Contents:**

1. PROLOG Programming : Familiarity with Declarative Style of Programming, using PROLOG (3 Labs sessions)
2. Implementation of Symbolic Mathematics using PROLOG
3. Fuzzy Logic –Building the basic Constructs in C++)
4. Implementations of Fuzzy Primitives on DSP6713 Processor
5. Experimentation with ROSE Rough SET Software
6. Assessment of Instability of Inconsistent information system (C/C++)
7. Fractal dimension computing (MATLAB/Python

## (LC) [EDE-19016] - Simulation Laboratory

| Teaching Scheme | Examination Scheme |
|---|---|
| Tutorial: 1 hr/week | Marks: 100 |
| Practical: 2 hrs/week | Credits: 2 |

**Course Outcomes**:

At the end of the course, students will demonstrate the ability to:

1. Understand and implement the parallel processing.
2. Analyse various parameters of different architectures of computer/processor.
3. Implement concepts of GRAPH theory.

**Course Contents:**

1. Creation and use of P-Threads using C programming.
2. Implementation of message passing interface using MPI.
3. Static and dynamic power estimation of cache memory of chip multiprocessor using CACTI Simulator.
4. Study and use of functional units of DSP processors
5. Generate a Random Directed Acyclic Graph for a given number of Edges.
6. Write program to generate random cyclic graph for given a given number of edges.
7. Checking connectivity of the graph using Breadth First Search.
8. Checking whether the graph is tree or not tree using Depth First Search.

## (LC) [EDE-19017]- Seminar

**Teaching Scheme**
Practical: 2 hrs/week

**Examination Scheme**
Marks: 100
Credits: 1

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Identify contemporary topics/concepts pertaining to Digital Designs, Embedded Systems and prepare documentation with improved substance.
2. Present the selected topic with superiority demonstrating good communication skills.

**Course Contents:**

**Selection of Topic:**

- Select a topic relevant to the stream of study with content suitable for M. Tech. level presentation. For selection topics refer internationally reputed journals. The primary reference should be published during the last two or three years.
- Some of the journals/publications suitable for reference are: IEEE/the IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication - Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain
- Get the topic approved by the seminar guide well in advance.

**Preparation of Presentation and Report:**

- In slides, list out key point only. You may include figures, charts equations tables etc. but not running paragraphs. Font size used should be at least 20.
- Figures should be very clear and possibly drawn by you using suitable software tools. There should be a slide on “Conclusion”.
- A report of the seminar should be prepared which should contain the following.
    - Title of the seminar.
    - Name and other details of presenter and the guide.
    - Abstract of the topic.
    - Contents such as Introduction, Theory to elaborate the concept, Implementation if carried out by the presenter/or fellow researcher/s, Comparison with other relevant techniques, Conclusion etc.
    - List of references strictly in IEEE format.

**Oral Presentation:**

- Student needs to orally present the topic for 20 minutes with good voice projection and with modest pace

**Answering Queries:**

Student needs to answer queries raised by the audience and evaluators. This session shall be restricted to 5 minutes. In case of more queries, student is supposed to solve the queries offline.

## SEMESTER II

### (IOC) [ETC-19004]- Embedded System Design

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Implement simple sketches on the Arduino boards involving several peripherals
2. Identify, design and implement applications on the Arduino boards producing custom shields.
3. Deploy low end applications using low and high level languages on microcontroller platform.

**Course Contents:**

**Introduction to Processors:** Introduction of Mkicroprocessors and Microcontrollers, Introduction of Arduino Microcontrollers.

**Introduction to Architecture**: Atmega328 : Basics and internal Architecture, Instruction Set

**Arduino Programming:** Arduino programming basics, Analog/Digital components and its application with Arduino , IDE for Arduino.

**Other Utilities in Arduino:** Timers, Analog comparators and hardware interrupts

**Interfacing with Peripherals:** Communication buses, Interfacing of I/O devices

**Case Studies:** Case studies of a few projects using Arduino boards and Shields

**References:**


1. Brian Evans, “Beginning Arduino Programming”, Springer, 2011
2. Michael J. Pont , “Embedded C”, Pearson Education, 2nd Edition, 2008
3. Raj Kamal, “ Embedded Systems – Architecture: Programming and Design”, TMH
4. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley


### (DEC-II) (a) [ETC(DE)-19007]- Automotive Electronics

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Design the digital control of drives using sensors and Digital Control Systems.
2. Design the starting and braking system for the automobiles.
3. Do research in field of automotive electrical applications.

**Course Contents:**

**Introduction**: Microprocessor and micro Computer applications in automobiles; components for engine management system, chassis system, motion control; electronic panel meters.

**Sensors & Actuators:** Different types of Sensors such as oxygen sensors, crank angle position sensors, fuel metering/vehicle speed sensors and detonation sensors, altitude sensors, flow Sensors, throttle position sensors, Solenoids, stepper motors, relays.

**CAN**: Architecture, Data transmission, Layers, Frame formats, applications Fuel Injection & Ignition System: Feedback carburettor system; throttle body injection and multi point fuel injection System; injection system controls; electronic spark timing.

**Engine Control System:** Open loop and closed loop control system; engine cooling and warm-up control; acceleration, deceleration and idle speed control; integrated engine control system; exhaust emission control engineering; on-board diagnostics; Automotive Electrical: Batteries; starter motor & drive mechanism; D.C. generator and alternator; lighting design; dashboard instruments; horn, warning system and safety devices.

**Comfort & Safety:** Seats, mirrors and sun roofs; central locking and electronic windows; cruise control; in-car multimedia; security; airbag and belt tensioners Electromagnetic Interference Suppression, Electromagnetic compatibility.

**References :**


1. John B. L Heywood, “Internal Combustion Engine Fundamentals”, Mc-GrawHill Inc.
2. Nicolas Navet, “ Automotive Embedded Systems Handbook”, edited by, CRC press
3. Williams Ribbens, “Understanding Automotive Electronics”, Elsevier Pub.
4. Ronald K. Jurgen “Automotive Electronics Handbook”, McGraw Hill Inc
5. “BOSCH CAN Specifications Version 2”.


## (DEC II) (b) [EDE(DE)-19002] - Pattern Recognition and Classification

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1 Analyze object description, recognition techniques, design and implement classification techniques,

2. Implement and compare the mathematical concepts of pattern recognition.
3. Apply AI techniques to object detection and classification.

**Course Contents:**

**Shape representation and description:** Region identification, contour based shape representation and description, chain codes, simple geometric border representation, Fourier transforms of boundaries, boundary description using segment sequences, B spline representation, other contour based shape description approaches, Shape invariants, Region based shape representation and description, Simple scalar region descriptors, moments, convex hull, graph based on region skeleton, region decomposition, region neighborhood graphs, shape classes.

**Mathematical morphology:** Basic morphological concepts, morphological principles, binary dilation and erosion, hit or miss transformation, opening and closing, gray scale dilation and erosion, thinning and skeletonization, gray scale dilation and erosion properties of erosion and dilation, opening and closing, top hat transformation, statistical texture description, methods based on spatial frequencies, co-occurrence matrices, edge frequency, other statistical methods of texture description.

**Knowledge representation and decision making:** Knowledge representation, statistical pattern recognition, classification principles, classifier setting, classifier learning, Baye‟s classification, nearest neighbor classification, cluster analysis. Artificial neural networks and fuzzy systems: Neural nets, feed forward networks, unsupervised learning, Hopfield neural nets, optimization techniques in recognition, genetic algorithms, simulated annealing, fuzzy systems, fuzzy sets and fuzzy membership functions, fuzzy set operators, fuzzy reasoning, fuzzy system design and training, Back propagation algorithm

**References:**


1. Richard Duda, Peter Hart, David Stork, “Pattern Classification”, Second Edition John Wiley and Sons Inc., 2005
2. Rajjan Shinghal, “Pattern Recognition: Techniques and Applications”, Oxford University Press, 2006.
3. Milan Sonka, Vaclav Hlavac, Roger Boyle, “Image Processing, Analysis, and Machine Vision” Brooks/Cole; 3rd edition (1 March 2007)
4. Madhuri A. Joshi, Mehul S. Raval, Yogesh H. Dandawate, Kalyani R. Joshi, Shilpa P. Metkar “Image and Video Compression: Fundamentals, Techniques, and Applications” CRC Press.


## (DEC-II) (c) [EDE(DE)-19010]- Blockchain Technology

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:
1. Learn the basics of cryptocurrency and blockchain

2. Grasp the complexities for applications of Blockchain in industrial world
3. Understand the emerging potentials of Blockchain technologies

**Course Contents:**

**Introduction to Digital Money-** Cryptocurrency, Cryptography Primitives, Bitcoins ecosystem,Storing, buying and selling bitcoins, IP packet versus block, WebApp versus DApp

**Architecture for Blockchain -** Hyperledger , Distributed ledger technology, Decentralized, Centralized and Distributed systems, Bitcoin versus Miulti-chain, Public and Private blockchain, Hard forks versus soft forks, Shrading side chains, Native blockchain tokens.

**Blockchain Platforms -** Ethereum, Ripple, Digiknow, Introduction to Blockchain programming using Javascript.

**Advanced concepts of Bitcoin- Blo**ckchain in Software Architecture, Analysis of Bitcoin protocol in networks

**Cybersecurity through Blockchain-** Current threat Landscape, Ransomware, Distributed Denial of Service.

**Industrial Applications-** Distributed ledger enabled IoT platforms

**References:**


1. The basics of Bitcoins and Blockchains-Antony Lewis
2. Blockchain: Transforming Your Business and Our World-Mark Van Rijmenam, Philippa Ryan
3. BLOCKCHAIN: From Concept to Execution- Debjani Mohanty
4. Blockchain for Dummies-Tiana Laurence, 2018


## (DEC –II) (d) [ETC(DE)-19001] - Automotive Embedded Hardware Development

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:
1 Acquire automotive specific hardware design skills
2. Understand concepts such as DFM, DFT, EMC, DFMEA
3. Apply processes, methods and tools to demonstrate design skills

**Course Contents:**

**Low Power Domain:** 16/32 bit controllers, Hardware-Software interfaces, Communication interfaces –

CAN, LIN, SPI, Wireless interfaces – Bluetooth, ISM band applications, I/O interfaces – digital, analog signal conditioning, switches, relays, high side, low side drivers, Introduction to design tools (Microcap, Cadence Concept HDL and Allegro)

**High Power Domain:** Selection of power switches devices – MOSFETs/IGBTs/SiC/GaNFETs, Gate driver design, power loss calculations, thermal management, Design considerations for High Voltage applications.

**Electromagnetic Compatibility:** Introduction to various regulatory requirements and International electrical and EMC standards, Understanding origin of pulses, disturbances, circuit and PCB layout design techniques to meet EMC.

**Design for Manufacturability and Testability:** PCB Layout considerations, Manufacturing interfaces and process flow, ICT, AOI and EOL testing.

**References:**

1. Online resources
2. Reference manuals from Hella-India

Note: Complementary lab session will be organized to ensure hands-on learning.

## (DEC– III) (a) [ETC(DE)-19008] - Low Power VLSI

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Identify the sources of power dissipation in digital IC systems and understand the impact of power on system performance and reliability.
2. Characterize and model power consumption and understand the basic analysis methods.
3. Understand leakage sources and reduction techniques.

**Course Contents:**

**Technology & Circuit Design Levels:** Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of $V_{dd}$ & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations

**Low Power Circuit Techniques:** Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

**Low Power Clock Distribution:** Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network.

**Logic Synthesis for Low Power estimation techniques:** Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers

**Low Power Memory Design:** Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits

**Low Power Microprocessor Design System:** Power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

**References:**


1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons Inc.,2000 .
3. J. B. Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.


## (DEC III) (b) [EDE(DE)-19005] - Multimedia Systems

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Understand the enabling mathematical techniques to study multimedia systems
2. Assimilate different compression principles and impact of specific hardware architectures
3. Grasp the complexities for deployment of multimedia systems, including security issues

**Course Contents:**

**Introduction to Multimedia**: Concepts, hypertext and hypermedia, Image, video & audio coding standards, digital audio & sound processing, elements of rate distortion theory, MIDI, Transmission of audio, MPEG-7, H.264.

**Mathematics for Multimedia**: Space and Linearity, Time and Frequency, Sampling and Estimation, Scale and Resolution, Redundancy and Information.

**Compression techniques**: Lossless compression, Lossy compression, MPEG compression standards,

Inter-frame and Intra-frame compression, fractal compression techniques, spatial & temporal redundancy, distortion theory, color image filtering, facial image segmentation,

**Animation**: Key frame animation techniques, morphing, animation and multimedia languages, animation using OpenGL, Multimedia authoring paradigms & user interfaces, VRML

**Architectures and Network Applications**: Array structure for motion estimation, Full-Search-Block-Matching-Algorithm, Application Specific Multimedia Processor Architecture for H.264 decoder, quantization & transmission of audio, network services & protocol for multimedia communications, multimedia over IP / ATM,

**Multimedia Retrieval and Protection:** Multimedia systems and databases, standards for meta-data, YouTube video format and metadata, content based retrieval in digital libraries, Internet multimedia content distribution, digital Items and digital rights management and security, Watermarking technique for multimedia protection, watermark detection, extraction, analysis of attacks

**References:**


1. The science of Digital media –Jeniffer Burg,
2. Mathematics for Multimedia-Mladen Victor Wickerhouser, Academic Press
3. Principles of Multimedia – Ranjan Parekh, TMH
4. Multimedia systems- John F. Bufford, Pearson
5. Multimedia system design – P.K Andeleigh
6. Multimedia Systems: Algorithms, Standards, Indus, practices- Parag Havaldar, Gerand Medioni
7. Graphics, GUI games and multimedia projects in C- Mahendra Pilania, Standard Publishers


## (DEC-III) (c) [EDE(DE)-19006]- Fault Tolerant & Dependable Computing Systems

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Understand the enabling techniques to study Fault tolerant systems
2. Assimilate different software principles and impact of reliability models
3. Grasp the complexities for fault tolerant and security issues

**Course Contents:**

**Hardware Fault Tolerance:** Fault, Error, Failure**,** Fault Classification, Types of Redundancy, Basic Measures of Fault Tolerance, Reliability evaluation techniques

**Network Fault Tolerance:** Traditional Measures, Network Measures, Canonical and Resilient Structures, Fault tolerance processor Level techniques, Preliminary Coding techniques, Graph Theoretical measures,

Fault Tolerant Routing

**Software Fault Tolerance**: Difference between Hardware and Software Fault tolerance, Bug Detection, Single version and N-version programming, Exception handling, Software Reliability Models

**Check pointing Techniques**: Introduction to Analytical model, Check pointing in distributed systems and shared-memory systems, forward and Backward Recovery, Data Replication and Resiliency

**Formal Methods for Safety in Critical Systems**: Industrial use of formal methods, Dependability assessment of embedded software systems, Managing fault tolerant design risks, Scheduling fault recovery operations for time critical applications, Energy efficient fault tolerant systems

**Modern Practices:** Defects Tolerance in VLSI Circuits**:** yield enhancement through redundancy, Simulation Techniques, Laser based fault injections in microcontrollers, Countermeasures against fault analysis techniques, Secure Coding.

**References:**


1. Fault Tolerant Systems- Israel Koren, C Mani Krishna, Elsevier, 2007
2. Fault Tolerant Computer System Design- D.K. Pradhan
3. Fault tolerant architectures for cryptography and hardware security- Sikhar Patranabis, D Mukhopadhya, Springer, 2018
4. Dependable Computing and Fault Tolerant Systems- A Avizienis, H Kopetz, C Laprie, pringer Verilag.
5. Advanced Concepts in Operating Systems- Singhal and Shivaratri
6. Fault Tolerance in Distributed Systems- Pankaj Jalote
7. Energy Efficient Fault Tolerant Suystems- Mathew Jimson, DK Pradhan, 2014
8. http://www.ecs.umass.edu/ece/koren/FaultTolerantSystems/simulator/


## (DEC – III) (d) [ETC(DE)-19002]- Automotive Embedded Software Development

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Acquire automotive specific software design skills
2. Understand concepts such as AUTOSAR, MATLAB, Communication Protocol
3. Apply processes, methods and tools to demonstrate design skills

**Course Contents:**

**Software Architecture:** Classical architecture, Layered Architecture (AUTOSAR), All layer information (e.g. RTE, BSW, Applications) Tool: Davinci developer, Configurator, Raphsody.

**Communication Protocols:** CAN, LIN, Automotive Ethernet, RF, Bluetooth, Wi-Fi, Diagnostic Protocols: UDS, Tools: CANoe, Vehicle spy, CAPEL, TAE scripting.

**Model Based Development:** Algorithm/application development using Simulink, Stateflow, Code generator.

**Embedded C:** Concept of C (structure, union, pointer, bitwise operator), Logic building according to requirement, MISRA C guidelines.

**Software Testing:** Unit testing, Model in loop (MIL) testing, Module testing, Integration testing, Software in loop (SIL) testing, Hardware in loop (HIL) testing, Tools: Tessy, Polyspace, TPT, Winidea, QAC, HIL test setup.

**References**:


1. Online resources
2. Reference manuals from Hella-India


Note: Complementary lab session will be organized to ensure hands-on learning.

## (LLC) - Liberal Learning Course

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 01

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Exhibit self learning capabilities and its use in effective communication.
2. Inculcate impact of various areas to relate with society at large.

**Course Contents:**

Identification of topic and resources, scope, and synthesize viewpoints for the areas such as performing arts, social sciences, business, philosophy, Agriculture sports and athletics, Fine Arts Medicine and Health Linguistics, defence studies and education.

## (PCC) [EDE-19002]- Embedded Systems Security

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

By the end of this course students will demonstrate the ability to:

1. Recognize vulnerabilities, attacks and need of protection mechanisms for embedded systems
2. Analyze and evaluate software vulnerabilities and attacks on operating systems
3. Identify terms/concepts relevant to embedded cryptography.
4. Develop and deploy solutions for security of embedded software and data protection.

**Course Contents:**

**Introduction to Embedded Systems Security:** Trends, Policies, Threats

**Systems Software Considerations:** Role of the Operating System, Multiple Independent Levels of Security, Microkernel versus Monolith, Core Embedded Operating System Security Requirements, Access Control and Capabilities, Hypervisors and System Virtualization, I/O Virtualization, Remote Management, Assuring Integrity of the TCB

**Secure Embedded Software Development:** PHASE—Principles of High-Assurance Software Engineering, Minimal Implementation, Component Architecture, Least Privilege, Secure Development Process, Independent Expert Validation, Case Study: HAWS—High-Assurance Web Server, Model-Driven Design

**Embedded Cryptography:** Cryptographic Modes, Block Ciphers, Authenticated Encryption, Public Key Cryptography, Key Agreement, Public Key Authentication, Elliptic Curve Cryptography, Cryptographic Hashes, Message Authentication Codes, Random Number Generation, Key Management for Embedded Systems, Cryptographic Certifications

**Data Protection Protocols for Embedded Systems:** Data-in-Motion Protocols, Data-at-Rest Protocols
**Emerging Applications:** Embedded Network Transactions, Automotive Security, Secure Android, Next-Generation Software-Defined Radio

**References:**


1. 1. David Kleidermacher and Mike Kleidermacher, “Embedded Systems Security”, Elsevier
2. Gebotys, Catherine H., “Security in Embedded Devices”, Springer
3. Stapko T., “Practical Embedded Security”, Elsevier/Newnes


## (PCC) [EDE-19003]- Real Time Operating Systems

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

By the end of this course students will demonstrate the ability to:

1. Describe the fundamental concepts of RTOS.

2. Explain various techniques for task management, inter task communication and synchronization.
3. Develop and analyze application software for embedded systems using the RTOS functions.

**Course Contents:**

Introduction to Embedded C, Difference between C & Embedded C Programming style, Basic structure of C program, RTOS Concepts: Foreground and background systems, Critical section, Shared Resources, Tasks, Multitasking, Context Switching, Kernels, Pre-emptive and non pre-emptive Schedulers, Static and Dynamic Priorities, Priority Inversion, Mutual exclusion, Synchronization, Inter task Communication mechanisms, Interrupts: Latency, Response and recovery, Clock Tick, Memory Requirements.

RTOS Kernel Structure: Tasks, Internal Tasks, Task States, TCB, Ready List, Task Scheduling, Task Level Context Switching, Locking and unlocking of scheduler, , Interrupt Management, Direct and Deferred Post Methods, Initialization, Starting the OS, Task Management, Time Management, Timer Management, Event Control Blocks, Synchronization in µCOS-II and µCOS-III - Semaphore Management, Mutual Exclusion Semaphores, Event Flag Management, Intertask Communication in µCOS-II and µCOS-III - Message Queue Management, Memory management, MCB, Porting of RTOS, Real Time Application.

**References:**


1. Jean Labrosse, " MicroC/OS-II The Real Time Kernel", CMP Books , 2nd Edition.
2. "µC/OS-III: The Real-Time Kernel for the Texas Instruments Stellaris MCUs"
3. David E. Simon, "An Embedded Software Primer", Addison-Wesley Professional, 1999.
4. Raj Kamal, "Embedded Systems – Architecture: Programming and Design", Tata McGraw-Hill Education, 2003.


## (PCC) [EDE-19004]- Digital CMOS VLSI Design

**Teaching Scheme**
Lectures: 3 hrs/week

**Examination Scheme**
T1, T2 – 20 marks each, End-Sem Exam – 60
Credits: 03

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Analyze, design, optimize and simulate simple and complex digital circuits using CMOS according to the design metrics.
2. Connect the individual gates to form the building blocks of a system.
3. Use EDA tools like Cadence, Mentor Graphics and other open source software tools

**Course Contents:**

**MOS Transistor Theory:** Physical structure of MOS transistor, MOS transistor under static conditions, secondary effects, SPICE models for MOS transistor, Process variation, Technology Scaling.

**The Manufacturing Process:** Manufacturing CMOS integrated circuits, design rules, packaging integrated

circuits, trends in process technology.

**CMOS Inverter:** CMOS inverter, Static and Dynamic behavior of CMOS inverter, Power, Energy and Energy-Delay, Technology Scaling and Impact on inverter Metrics.

**Combinational Logic Designs in CMOS**: Static CMOS design, Dynamic CMOS Design, Examples.

**Sequential Logic Designs in CMOS**: Introduction, Static latches and registers, Dynamic latches and registers, Pipelining, Examples.

**Designing Arithmetic Building Blocks:** Adders, Multipliers, Shifters, Power and Speed Trade-Off in Data path Structures

**References:**


1. Jan Rabaey, Anantha C , Borivoje Nikolic "Digital integrated circuits- A design perspective", 2nd edition, PHI.
2. Kamran Eshraghian, Pucknell and Eshraghian, "Essentials of VLSI Circuits and Systems", Prentice-Hall (India).
3. Kang, Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", TATA McGRAW Hill.
4. Wayne Wolf, "Modern VLSI Design", Pearson Education.
5. Neil Wieste, David Harris, Ayan Banerjee, "CMOS VLSI Design", 3rd Edition, Pearson Education, 2008.


## (LC) [EDE-19005]- Real Time Operating System Laboratory

**Teaching Scheme**
Lectures: 2 hrs/week

**Examination Scheme**
Marks: 100
Credits: 01

**Course Outcomes:**

By the end of this course students will be able to:

1. To program an embedded system with multitasking concepts.
2. Demonstrate Task Management.
3. Demonstrate Inter-Task Communication.

**Course Contents:**

1. Controlling of peripherals without using µC/OS -II services.
2. Study of Task creation using OSTaskCreate()
3. Study of Task creation using OSTaskCreateExt()
4. Exploring multitasking features of µC/OS -II.
5. Study of Semaphore Service of µC/OS -II.
6. Study of Mutex Service of µC/OS -II.
7. Exploring Mailbox management Services of µC/OS -II.
8. Exploring Message Queue Services of µC/OS -II.
9. Real Time Application Development using µC/OS –II services.

## (LC) [EDE-19006]- Digital CMOS VLSI Design Laboratory

**Teaching Scheme**
Lectures: 2 hrs/week

**Examination Scheme**
Marks: 100
Credits: 01

**Course Outcomes:**

At the end of the course, students will demonstrate the ability to:

1. Understand Digital Circuit design using CMOS.
2. Build blocks of a system to solve engineering problems.
3. Use EDA tools like Cadence, Mentor Graphics and other open source software tools like NGSPICE through lab exercises.

**Course Contents:**

1. SPICE simulation of basic analog circuits.
2. Analog Circuit simulation using Cadence tools
3. Verification of layouts (DRC, LVS)
4. Back annotation

## (LC) [EDE-19007]- Embedded Systems Security Laboratory

**Teaching Scheme**
Lectures: 2 hrs/week

**Examination Scheme**
Marks: 100
Credits: 01

**Course Outcomes:**

1. Build the basic blocks of crypto algorithms using Verilog
2. Implement the crypto algorithms on reconfigurable platforms

**Course Contents:**

1. Simulate the Giffe generator using Verilog/VHDL (using 2 to 1 Multiplexer).
2. Grain-128 design is based on the concept of Control path and Data path. Draw the block diagram of Grain-128 data path showing LFSR and NFSR. Write Verilog code
3. Draw a schematic block diagram of f-Function used in DES rounds. Write Verilog/VHDL code for description in entity architecture format. State your assumptions.
4. Describe Entity / Architecture description using Verilog/VHDL constructs for overall DES hardware realization. Support your answer with one to one schematic diagram.
5. Exploring the security features of partial reconfiguration in XILINX Platform.